REMARKS

I. Introduction

In conjunction with the Request for Continued Examination (RCE) for the above-entitled application, and response to the Office Action dated January 29, 2002, which was made Final, claims 19, 28, and 37, have been amended; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii), and claims 46-70 have been added. Claims 19, 21-28, 30-45, and 46-70 are in the application. Entrance of these amendments prior to the examination of the RCE, examination, and re-consideration of the application, as amended, are respectfully requested.

II. Art-Based Rejections

In pages 2-4, the Office Action rejected claims 19, 21-28, and 30-45 under 35 U.S.C. § 103(a) as being unpatentable over Zhang (USPN 5,717,224) in view of Lien et al (USPN 5,309,264).

The Applicants respectfully traverse the rejections, and in order to expedite prosecution, have amended the claims in order to overcome the rejections and place the application in order for allowance.

A. The Zhang Reference

The Zhang reference discloses a channel forming region of a thin film resistor being covered with an electrode and wiring line that extends from a source line. As a result, the channel forming region is prevented from being illuminated with light coming from above the thin-film transistor, whereby the characteristics of the thin-film transistor can be made stable. See Abstract.

B. The Lien et al Reference

The Lien et al reference discloses a liquid display comprising a first substrate having a plurality of electrodes thereon, a second substrate having a common electrode, and a liquid crystal material disposed between the first substrate and the second substrate. See Abstract. The bottom pixel electrode is a continuous square, although separated on all sides from adjacent pixel electrodes of the same type by gate and data bus lines, while the portion of the common electrode which forms the top pixel electrode has an "X" shaped cutout formed therein with the ends thereof pointing at the corners of the pixel. See Col. 4, lines 1-8, and FIG. 2. The direction of the electric field around the periphery of the pixel and at the edge of the cutout is such that each pixel is divided into four domains. In each domain the director of the liquid crystal display molecules is always aligned so as to tilt in a direction toward the center of the pixel when an electric field is applied (as opposed to being perpendicular to the substrates when there is no electric field applied). However, the X shaped cutout defines the boundaries of four distinct liquid crystal domains I, II, III, and IV. See Col. 4, lines 20-31.

C. The Claims are Patentable over the Cited References

The present invention is directed towards liquid crystal displays. An apparatus in accordance with the present invention comprises a first substrate, a plurality of gate lines and drain lines formed on the first substrate, and thin film transistors that are arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source. The apparatus further comprises an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines, a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding gate line extending in a row direction, a second substrate disposed

opposite the first substrate, a liquid crystal layer arranged between the first and second substrates, a common electrode formed on the second substrate, and an orientation control window created in the common electrode; wherein orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and the interlayer insulation film has a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines. The amendments to the claims are supported by FIGS. 16-21, as well as the discussion related thereto, and the discussion and drawing of FIG. 3 of the present invention.

The cited references do not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited references do not teach nor suggest the element of overlapping the pixel electrode is with the corresponding gate line extending in a row or column direction as claimed in independent claims 19, 28, 37, and 46. As such, independent claims 1, 5, 10, 11, 13, and 16 are patentable over the Zhang and Lien references.

The Zhang reference does not teach that the pixel electrode (reference numeral 510 in Zhang) overlaps the corresponding gate line (gate electrode 504 in Zhang) in a row or column direction. Further, Zhang shows that the pixel electrode 510 specifically does not overlap the corresponding gate line in FIG. 5, as well as in FIG. 4A and 4B. Zhang also does not discuss overlapping the pixel electrode with the corresponding drain line extending in either a row or column direction, since no row or column directions are discussed in Zhang.

The ancillary Lien et al reference does not remedy the deficiencies of the Zhang reference, namely, Lien does not teach nor suggest the element of overlapping the pixel electrode is with the corresponding drain line extending in a row or column direction as claimed in independent claims 19, 28, 37, and 46. Further, Lien teaches away from any such overlap, since Lien specifically states that the lines are adjacent to the electrodes, not overlapped with them, in Col. 4,

lines 1-3: "the bottom pixel electrode is a continuous square (although separated on all sides from adjacent pixel electrodes of the same type by gate and data bus lines...)." As such, Lien teaches away from the claimed overlap, and cannot be combined with Zhang to show the claimed element of overlapping the pixel electrode is with the corresponding drain line extending in a row or column direction as claimed in independent claims 19, 28, 37, and 46.

Dependent claims 21-28, 30-36, 38-45, and 47-53 are also likewise patentable over the cited references, because they contain all of the limitations of the independent claims. Further, the dependent claims recite additional novel elements which further distinguishes them from the cited references.

III. Conclusion

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectively solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

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APPENDIX A: CLAIMS IN MARKED-UP FORM

19. (Twice Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding gate line extending in a row direction;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and the interlayer insulation film has a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

21. (Unchanged) The liquid crystal display as claimed in claim 19, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

22. (Unchanged) The liquid crystal display as claimed in claim 19, wherein the interlayer insulation film has a thickness of at least 1 μm.

23. (Unchanged) The liquid crystal display as claimed in claim 19, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

24. (Unchanged) The liquid crystal display as claimed in claim 19, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

25. (Unchanged) The liquid crystal display as claimed in claim 24, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

26. (Unchanged) The liquid crystal display as claimed in claim 24, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

27. (Unchanged) The liquid crystal display as claimed in claim 24, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

28. (Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, wherein the interlayer insulation film has a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

30. (Unchanged) The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

31. (Unchanged) The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness of at least 1 μm.

32. (Unchanged) The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

33. (Unchanged) The liquid crystal display as claimed in claim 28, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

34. (Unchanged) The liquid crystal display as claimed in claim 33, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

35. (Unchanged) The liquid crystal display as claimed in claim 33, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

36. (Unchanged) The liquid crystal display as claimed in claim 33, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

37. (Unchanged) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and a plurality of drain lines formed on the first substrate and defining a plurality of pixels;

a thin film transistor for each pixel formed on the first substrate, the thin film transistor having a gate electrode connected to the corresponding gate line, a drain electrode connected to the corresponding drain line, and a source electrode;

an interlayer insulation film formed over the thin film transistors, the gate lines, and the drain lines;

a pixel electrode for each pixel, the pixel electrode being connected to the source electrode of the corresponding thin film transistor and at least partially formed on the interlayer insulation film;

a second substrate disposed opposite the first substrate;

a liquid crystal layer filled between the first and second substrates; and

a common electrode formed on the second substrate, wherein the common electrode defines an orientation control window disposed across the liquid crystal layer from each pixel, the orientation control window being a region on the second substrate free of the common electrode.

38. (Amended) The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness sufficient to alleviate an influence on the liquid crystal layer by an electric field generated by the thin film transistors, the gate lines, and the drain lines.

39. (Unchanged) The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

40. (Unchanged) The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness of at least 1 μm.

41. (Unchanged) The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

42. (Unchanged) The liquid crystal display as claimed in claim 37, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

43. (Unchanged) The liquid crystal display as claimed in claim 42, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

44. (Unchanged) The liquid crystal display as claimed in claim 42, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

45. (Unchanged) The liquid crystal display as claimed in claim 42, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

46. (New) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a column direction;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and the interlayer insulation film has a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

47. (New) The liquid crystal display as claimed in claim 46, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

48. (New) The liquid crystal display as claimed in claim 46, wherein the interlayer insulation film has a thickness of at least 1 μm.

49. (New) The liquid crystal display as claimed in claim 46, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

50. (New) The liquid crystal display as claimed in claim 46, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

51. (New) The liquid crystal display as claimed in claim 50, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

52. (New) The liquid crystal display as claimed in claim 50, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line